

Bottom-up approach self-assembly of nanoscale object via self-organisation.

Top-down approach making micro- and nanometre-scale devices by growing layered materials and patterning bulk materials.

due to the quantum effects in the electronic system.

Nano- and micro-electronic systems / devices

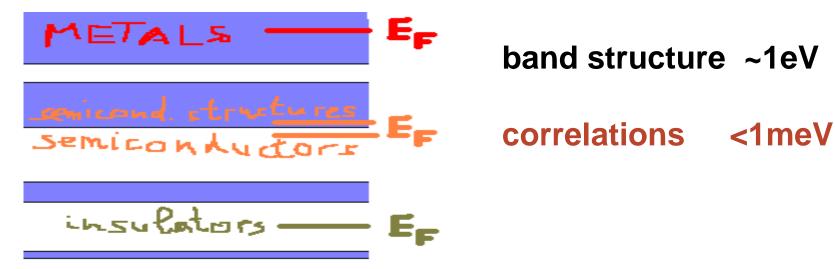
Top-down manufacturing methods: growth and lithography. Use of AFM for nanoprocessing. Lithographically defined one-dimensional wires in semiconductors. Electronics =

#### electronic transport + sensitivity of transport characteristics to external conditions: magnetic field, temperature, electromagnetic environment.

**Electronics materials:** 

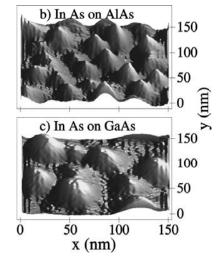
Semiconductors and semiconductor heterostructures Normal and Ferromagnetic metals, Superconductor

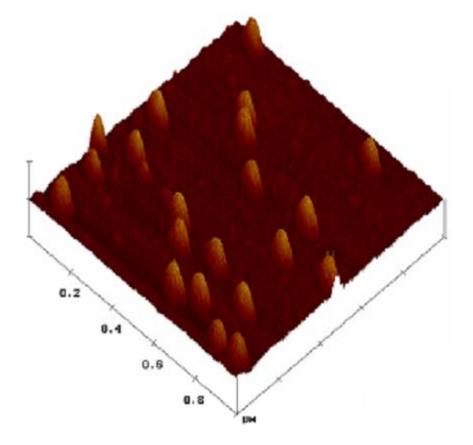
Electron dynamics in each material is determined by



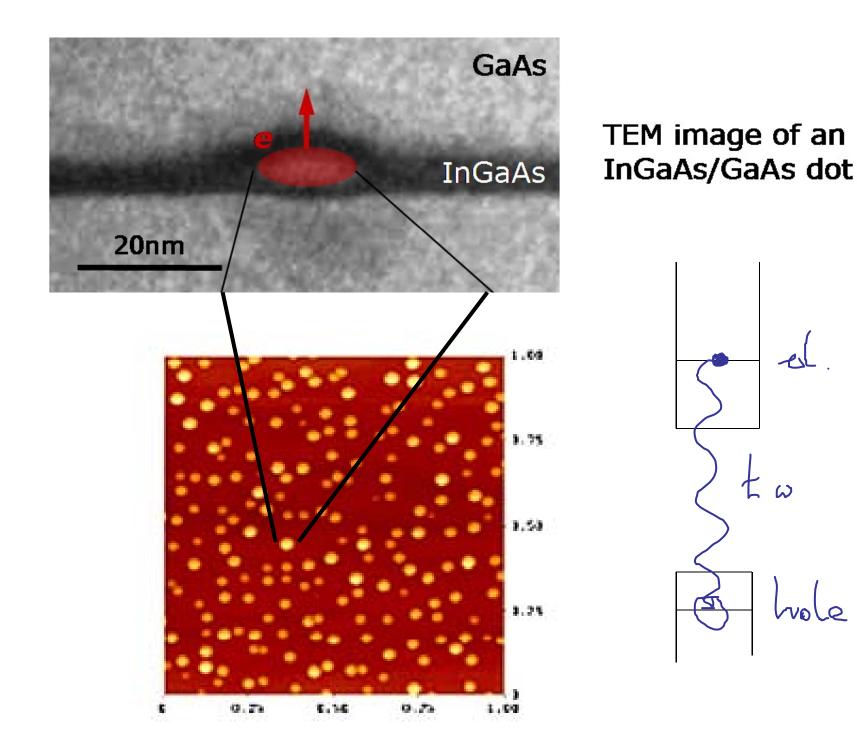
# **Self-assembled semiconductor dots**

Due to lattice mismatch between two semiconductor materials, dots of one material tend to form, by themselves, on the surface of another: 'self-organisation'.

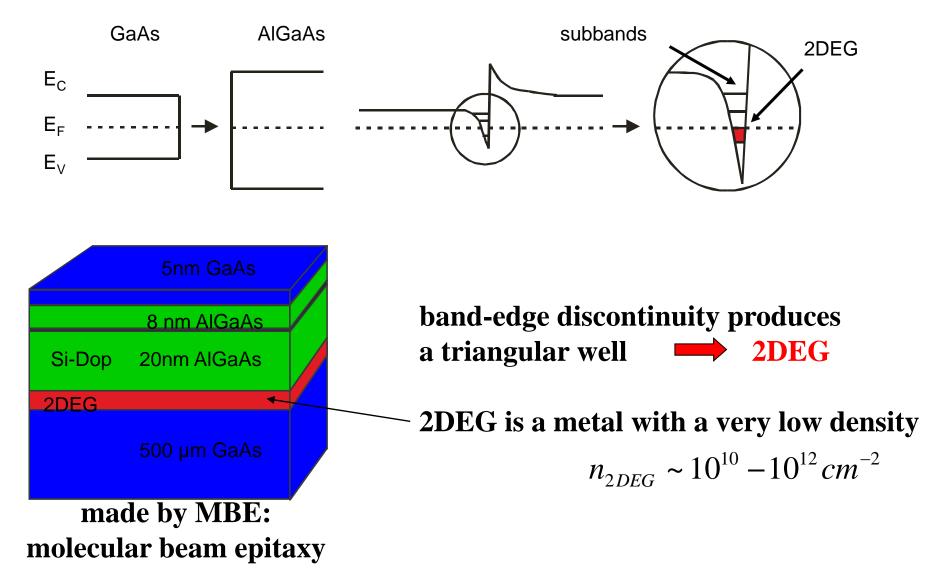


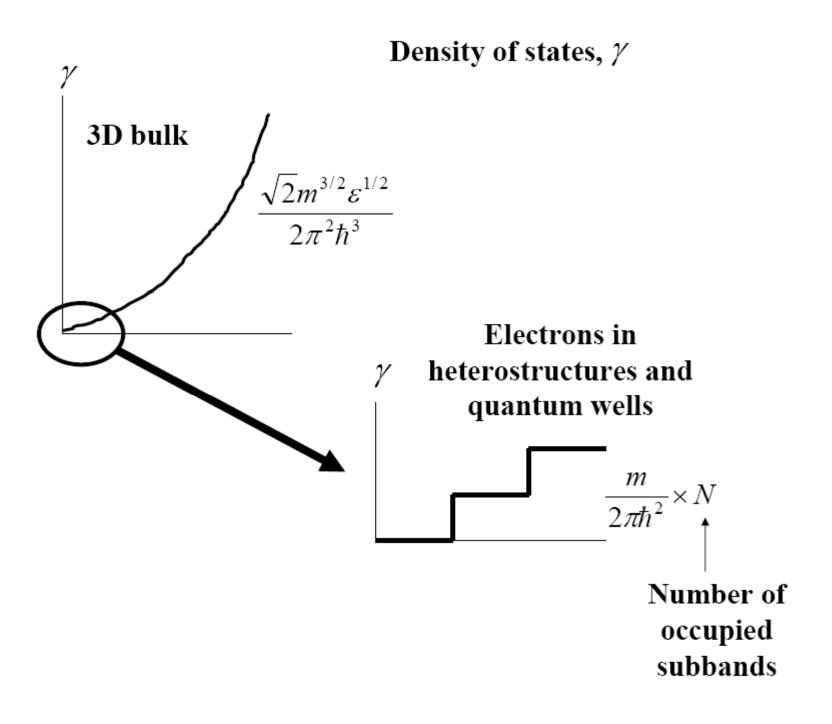


InP dots formed on the GaInP surface (AFM scan)

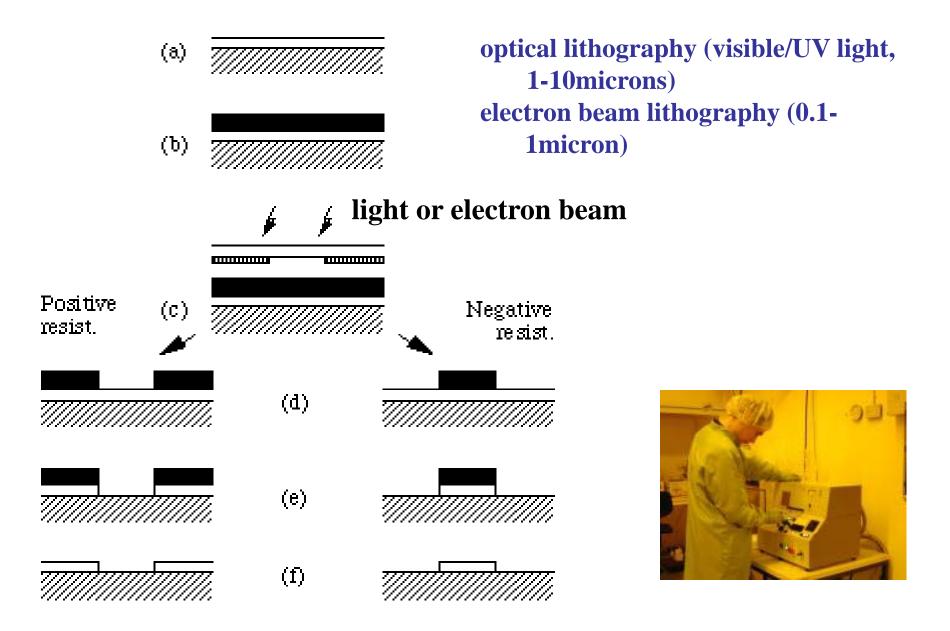


# **Semiconductor Heterostructures**



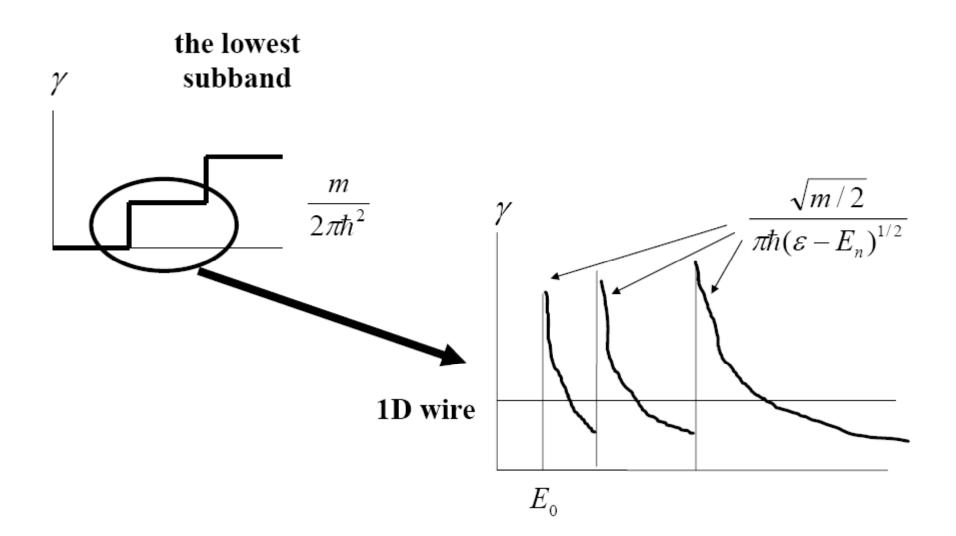


## How to make micro/nanotructures: wires and dots



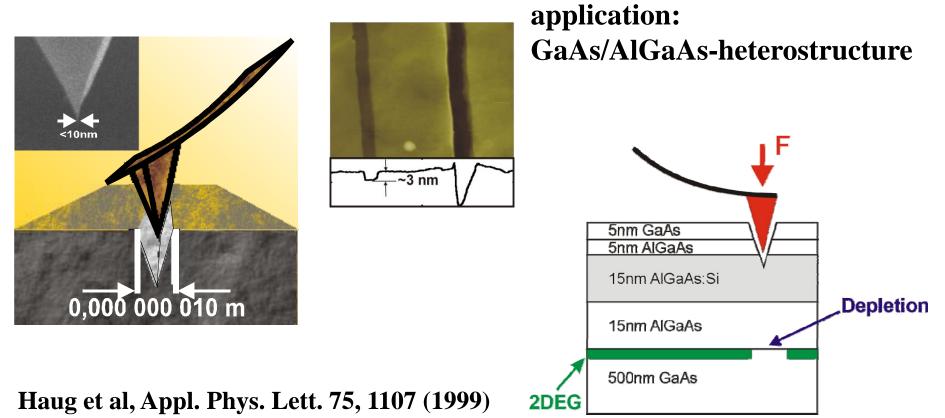
#### Making quasi-one-dimensional wires using lithographically processed metallic gates Top-gate V<sub>TG</sub>. 500nm |} Polyimide Split-gate SG 10nm 돶 GaAs 2DEG AlGaAs 100nm GaAs ≈ ≈

Density of states,  $\gamma$ 

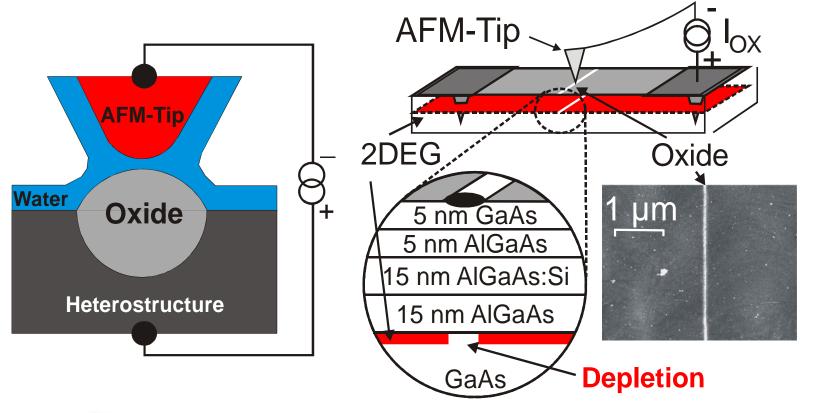


# Surface Modification (direct writing) with an AFM (10-100nm)

#### nanomachining



## Local Oxidation (10-100nm)



Ishii, Matsumoto (1995), Held et al. (1998)

